Amendments to the Claims

The following listing of claims replaces all prior versions and listings of claims:

1. (Currently amended) Byte alignment circuitry comprising:

a data input;

a control input;

a special character selection input indicating which one of a plurality of different special ~~character~~ characters is to be used for byte alignment, the plurality of different special characters including special characters having a plurality of different sizes in terms of how many bytes they include; ~~and~~

a special character status output indicating which one of the plurality of special ~~character~~ characters was used to align the byte boundaries; and

a data output.

2. (Original) The circuitry defined in claim 1 wherein said data input is one of a plurality of parallel data inputs.

3. (Currently amended) The circuitry defined in claim 2 wherein said plurality of parallel data inputs is the number of bits in a byte.

4. (Original) The circuitry defined in claim 1 wherein said data output is one of a plurality of parallel data outputs.

5. (Currently amended) The circuitry defined in claim 4 wherein said plurality of parallel data outputs is the number of bits in a byte.

6. (Original) The circuitry defined in claim 5 wherein successive aligned bytes are output one after another via the data outputs.

7. (Original) The circuitry defined in claim 1 further comprising a clock input.

8. (Original) A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

byte alignment circuitry as defined in claim 1 coupled to said processing circuitry and said memory.

9. (Original) A printed circuit board on which is mounted byte alignment circuitry as defined in claim 1.

10. (Original) The printed circuit board defined in claim 9 further comprising:

a memory mounted on said printed circuit board and coupled to said byte alignment circuitry.

11. (Original) The printed circuit board defined in claim 9 further comprising:

processing circuitry mounted on said printed circuit board and coupled to said byte alignment circuitry.

12. (Currently amended) Circuitry for receiving and byte-aligning data comprising:

byte alignment circuitry that uses a first special character selected by a special character selection signal from a plurality of different special characters having a plurality of different sizes in terms of how many bytes they include to detect byte boundaries in received data, and aligns the byte boundaries when enabled by a control signal to subsequently output byte-aligned data and a special character status signal indicative of which one of the special ~~character~~ characters was used to align the byte boundaries; and

utilization circuitry responsive to outputs of the byte alignment circuitry and selectively providing said control signal and said special character selection signal.

13. (Original) The circuitry defined in claim 12 wherein the byte-aligned data is output in parallel form.

14. (Original) The circuitry defined in claim 12 wherein said utilization circuitry comprises programmable logic circuitry.

15. (Original) The circuitry defined in claim 12, wherein said byte alignment circuitry outputs a pattern detect signal indicative of the presence of byte aligned data; and

said pattern detect signal causes said utilization circuitry to disable said control signal.

16. (Original) The circuitry defined in claim 12, wherein said byte alignment circuitry automatically prevents alignment to subsequently received data containing byte boundary data after the byte boundaries have already been aligned.

17. (Original) The circuitry defined in claim 12, wherein said byte alignment circuitry provides data representing said first special character to said utilization circuitry.

18. (Currently amended) The circuitry defined in claim 12, wherein said special character select signal can instruct said byte alignment circuitry to use a second special character selected from the plurality of different special characters to detect the byte boundaries in received data.

19. (Original) The circuitry defined claim 18, wherein said byte alignment circuitry re-aligns the byte boundaries using said second special character when enabled by said control signal.

20. (Currently amended) Circuitry for receiving and byte-aligning data comprising:

byte alignment circuitry that processes received data and outputs byte-aligned data after byte boundaries are aligned, said byte alignment circuitry further comprising:

special character detection circuitry that detects a selected special character in the received data, said selected special character ~~is~~ being selected, based on a selection signal, from a plurality of different special characters that have a

plurality of different sizes in terms of how many bytes they include; and

boundary adjustor circuitry that sets the byte boundaries when said selected special character is detected and criteria are met; and

utilization circuitry that receives the outputs of said byte alignment circuitry.

21. (Currently amended) The circuitry defined in claim 20, wherein said selection signal is hardwired to permanently select a particular ~~selected~~ one of the special ~~character~~ characters from the plurality of different special characters.

22. (Currently amended) The circuitry defined in claim 20, wherein said utilization circuitry provides said selection signal to select a particular special character from the plurality of different special characters.

23. (Original) The circuitry defined in claim 20, wherein said byte alignment circuitry disables said boundary adjustor circuitry independent of a control signal.

24. (Original) The circuitry defined in claim 20, wherein said utilization circuitry enables said boundary adjustor circuitry by providing a control signal to said byte alignment circuitry.

25. (Currently amended) The circuitry defined in claim 20, wherein said byte alignment circuitry further ~~comprising~~ comprises special character constructor circuitry.